WHAT IS CLAIMED IS:

1. A solid-state image pickup element comprising:

a plurality of pixel blocks each having a plurality of photoelectric conversion elements, a plurality of transfer switches for transferring signals from said respective photoelectric conversion elements, and a common amplifier for receiving signals from said plurality of transfer switches; and

a scanning circuit for outputting a scanning clock for each pixel block.

2. An element according to claim 1, wherein said scanning circuit includes a shift register.

3. An element according to claim 1, wherein said scanning circuit includes a decoder.

4. An element according to claim 1, further comprising an operation processing circuit for receiving a plurality of transfer clocks corresponding to said plurality of transfer switches in said pixel block, performing operation processing for the scanning clock output from said scanning circuit and the plurality of transfer clocks, and supplying processed signals as clocks for driving said plurality of transfer switches.

5. An element according to claim 4, further comprising a decoder for converting one transfer clock input into a plurality of transfer clock inputs corresponding to said plurality of transfer switches in said pixel block and inputting the plurality of transfer clock inputs to said operation processing circuit.

6. An element according to claim 4, wherein said operation processing circuit includes an AND operation processing circuit for receiving the scanning clock and the transfer clock.

7. An element according to claim 5, wherein said operation processing circuit includes an AND operation processing circuit for receiving the scanning clock and the transfer clock.

8. An element according to claim 4, wherein said operation processing circuit includes an OR operation processing circuit for receiving the scanning clock and the transfer clock.

9. An element according to claim 5, wherein said operation processing circuit includes an OR operation processing circuit for receiving the scanning clock and the transfer clock.

10. An element according to claim 4, wherein

when said plurality of transfer switches of said pixel block are set as a plurality of first transfer switches, said operation processing circuit is formed from a plurality of second transfer switches,

the scanning clock is input to gates of said plurality of second transfer switches, and

the transfer clock inputs are supplied to said first transfer switches via said second transfer switches.

11. An element according to claim 5, wherein

when said plurality of transfer switches of said pixel blocks are set as a plurality of first transfer switches, said operation processing circuit is formed from a plurality of second transfer switches,

the scanning clock is input to gates of said plurality of second transfer switches, and

the transfer clock inputs are supplied to said first transfer switches via said second transfer switches.

12. An element according to claim 1, further comprising:

a reset switch arranged in each pixel block to reset a signal input portion; and

an operation processing circuit for receiving a reset clock input, performing arithmetic processing for the scanning clock and the reset clock input, and supplying a processed signal as a clock for driving said reset switch.

13. An element according to claim 1, further comprising:

a selection switch arranged in each pixel block to select said pixel block; and

an operation processing circuit for receiving a selection clock input, performing arithmetic processing for the scanning clock and the selection clock input, and supplying a processed signal as a clock for driving said selection switch.

14. An image pickup apparatus comprising:

said solid-state image pickup element defined in claim 1;

an optical system for forming light into an image on said solid-state image pickup element; and

a signal processing circuit for processing an output signal from said solid-state image pickup element.